

Sub B1

1. An interrupt request controller for processing a plurality of interrupt logic signals, such controller, comprising:

 a programmable bit masking section fed by the interrupt logic signals, adapted to mask selected ones of the interrupt signals;

 a interrupt priority section fed by the programmable mask section for coupling unmasked ones of the interrupt signals to a plurality of outputs selectively in accordance with a predetermined priority criteria.

2. An interrupt request controller for processing a plurality of interrupt logic signals, such controller, comprising:

 a programmable section fed by the interrupt signals, for selecting assertion sense and/or assertion type of each one of the interrupt signals.

3. An interrupt request controller for processing a plurality of interrupt logic signals, such controller, comprising:

 a programmable section fed the interrupt signals, for storing a bit for each one of the interrupt logic signals representative of whether the logic state of the interrupt logic signal should be, or should not be, inverted and for producing a corresponding output logic interrupt signal in accordance therewith.

4. An interrupt request controller for processing a plurality of interrupt logic signals, such controller, comprising:

 a programmable section fed the interrupt signals, for storing a bit for each one of the interrupt

6 ~~logic signals representative of whether the logic state of~~
7 the interrupt logic signal should remain as an edge or be
8 converted to a level and for producing a corresponding
9 output logic interrupt signal in accordance therewith.

1 5. An interrupt request controller for processing a
2 plurality of interrupt logic signals, such controller,
3 comprising:

4 a programmable section fed by the interrupt
5 signals, for selecting assertion sense and/or assertion type
6 of each one of the interrupt signals;

7 a programmable bit masking/section coupled to
8 the programmable assertion sense/assertion type section,
9 adapted to mask selected ones of the interrupt signals;

10 a interrupt priority section fed by the
11 programmable mask section for coupling unmasked ones of the
12 interrupt signals to a plurality of outputs selectively in
13 accordance with a predetermined priority criteria.

6. The interrupt request controller recited in claim 5 wherein the programmable assertion sense and/or assertion type section includes for each one of the interrupt logic signals an interrupt sense register for storing a bit representative of whether the logic state of the interrupt logic signal should be, or should not be, inverted.

1 7. The interrupt request controller recited in
2 claim 6 wherein the programmable assertion sense and/or
3 assertion type section includes for each one of the
4 interrupt logic signals, an interrupt type register for
5 storing a bit representative of whether the logic state of

- 6 ~~The interrupt logic signal should remain as an edge or be~~
7 ~~converted to a level.~~

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